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Simulation of 64-bit MAC Unit using Kogge Stone Adder and Ancient Indian Mathematics

Aapurva Kaul*, Abhijeet Kumar**
**(PG Scholar, Department of Electronics and Communication, MMU University, Haryana*
*** (Assistant Professor, Department of Electronics and Communication, MMU University, Haryana*

ABSTRACT
This paper describes that multiply and accumulate (MAC) unit plays a very vital role in various Digital Signal Processing applications. Speed of these applications depends on the speed of these three sub units of MAC multiply unit, adder unit and accumulator unit. In this paper the delay of 64-bit MAC unit is decreased as compared to the previous MAC units. In this Kogge Stone Adder is used as adder in design Vedic Multiplier using Urdhva Tiryakbhyam sutra. The designing of MAC unit is done under VIRTEX-4 family, XC4VFX140 device, FF1517 package and -11 speed and comparison of proposed MAC unit design is done under SPARTAN-3E family, XC3S500 device, FG320 package and -5 speed in Xilinx ISE 8.1i. The combinational path delay of the 64-bit MAC unit is 59.705ns in SPARTAN-3E family. Ancient Indian mathematics is being used for designing of multiplier unit to decrease the overall delay of the MAC unit.

Keywords- Accumulator, Kogge Stone Adder, Multiply and accumulate unit, Urdhva Tiryakbhyam, Vedic Multiplier.

I.INTRODUCTION

MAC unit consist of accumulator unit which is a combination of one multiplier unit and one adder unit. Delay in the system is generated by the long multiplication process and propagation delay is generated because of the parallel addition stages [1].In many digital signal processing applications MAC unit is an inevitable component. This unit is mainly used as it reduces the load of CPU by working independently [2]. In digital designs MAC operation is the vital computational operation and it also determines the speed of the processor. For reducing the delay of the processor various methods are being used including various types of adder units [3]. Applications where MAC unit is extensively used are discrete fourier transform, filtering, convolution, discrete wavelet transform, correlation etc. There are two vital factors which can be used in increasing the speed of the MAC unit. First one is reduction of partial products in multiplication unit and second is accumulator [4], [5].

This paper is divided into seven sections. First section is introduction, second section consist of discussion about MAC operation, third section consist of Vedic multiplier details, fourth section describes about Kogge stone adder, fifth section is obtained results, sixth section is comparison and in final seventh section conclusion is made.

II. MAC OPERATION

MAC unit is multiply and accumulate unit in this the multiplier unit is provided by the input values from the memory and then the generated output of the multiplier is provided to the adder unit and the output generated of the multiplier and the previous accumulator output are added in the adder and the output generated is stored in the accumulator. Accumulator used is a parallel in parallel out (PIPO) unit [6]. MAC operation can be explained by equation (1):

$$Z=A*B+Z \quad \ldots\ldots\ldots\ldots (1)$$

Where the multiplier A and multiplicand B have n bits each and end Z has (2n+1) bits [6].

Summation unit is the core of MAC unit as it consumes most of the power, area and delay. The proposed design of MAC unit is shown in Fig 1:

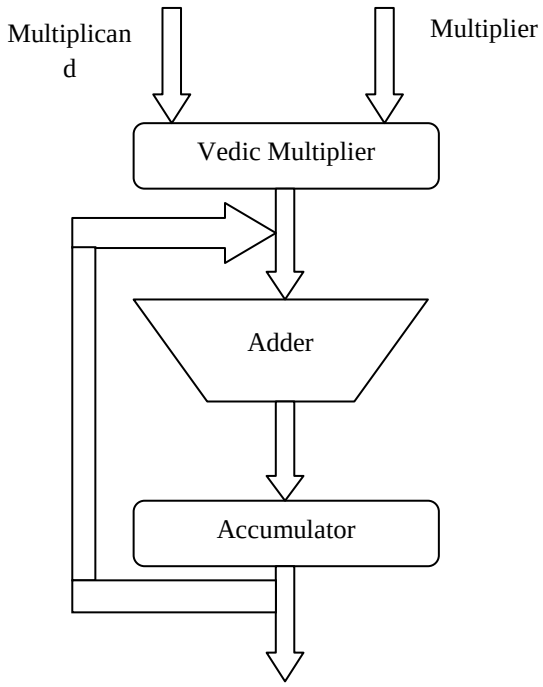


Fig 1: Proposed MAC unit

In 64-bit MAC unit the input provided to the Vedic multiplier are of 64-bit each and the output generated by the accumulator is 129-bit i.e. one bit for carry (128 bits + 1 bit) [7].

III. VEDIC MULTIPLIER

In this paper multiplier is being designed using ancient Indian mathematics as it reduces the partial products and area and also increases the speed hence decreases the delay of the MAC unit [1]. In this Urdhva Tiryagbhyam sutra i.e. vertically and Crosswise multiplication is used for multiplication of two binary numbers. In this partial product generation and addition are concurrently done hence delay is reduced [7]. The Urdhva Tiryagbhyam sutra is part of Sathapatya Veda (book on architecture and engineering), which is upaveda of Atharva Veda. There are 16 sutras and 16 Upasutras of Atharva Veda [8]. In the multiplication step 1 is multiplication of LSB numbers, step 2 is crosswise multiplication of LSB and MSB of the two digits and then the two outputs are adder and step 3 is multiplication of the MSB's and finally the final output of all the steps are added to generate the final output. The multiplication of two 2-bit binary numbers is shown in Fig 2:

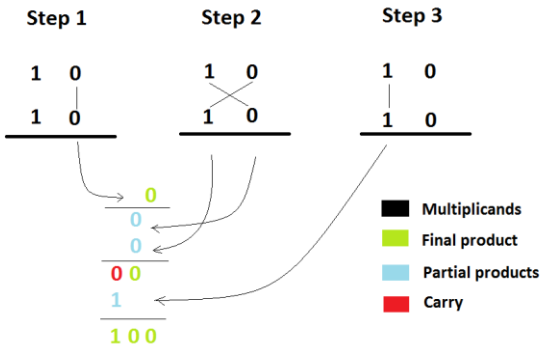


Fig 2: Multiplication of two 2-bit numbers [4]

For a 32-bit Vedic multiplier two 16-bit input's a and b are provided to 16-bit multiplier and then the outputs of these multipliers are added using Kogge stone adder and the final output of 32-bit multiplier is generated as q(63-32),q(32-16 and q(15-0) i.e. a 64-bit final output is generated. Block diagram of 32-bit multiplier is shown in Fig 3:

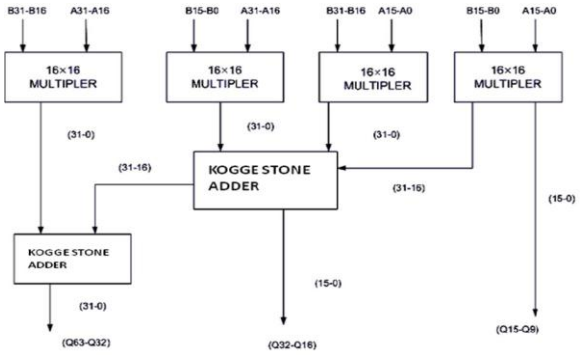


Fig 3: Block diagram of 32-bit Vedic multiplier [1]

IV. KOGGE STONE ADDER

Kogge stone adder generates and propagates signals or outputs in advance hence it is a parallel prefix adder. It is the fastest adder and it generates lowest delay. In this adder there are various blocks such as generate and propagate block, grey cell, black cell and sum block [9]. The block diagram of 8-bit Kogge stone adder is shown in Fig 4:

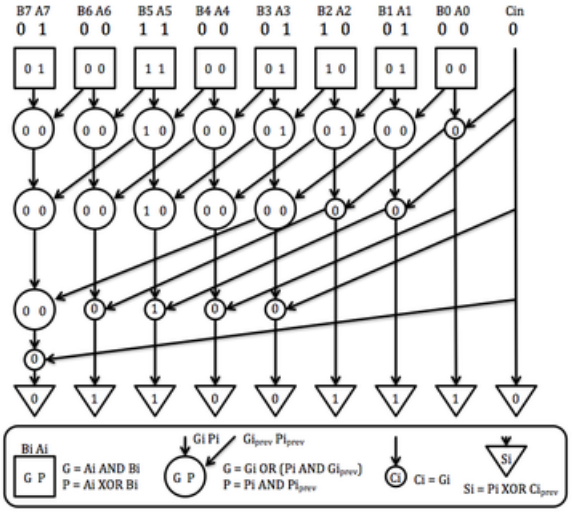


Fig 4: 8-bit Kogge Stone Adder [9]

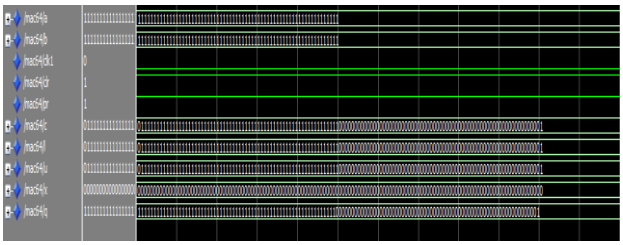
V. RESULTS

In this section, the result of the Kogge stone adder, Vedic multiplier and MAC unit are displayed using VIRTEX-4 family, XC4VFX140 device, 11FF1517 package, -11 speed. Design summary of 64-bit MAC unit is displayed in Fig 5 (a), it contains the number and percentage of slices, LUT's, IOB's and CLK's used by the unit, simulation output of 64-bit MAC unit is displayed in Fig 5 (b) and RTL view of 64-bit MAC unit is shown in Fig 5 (c):

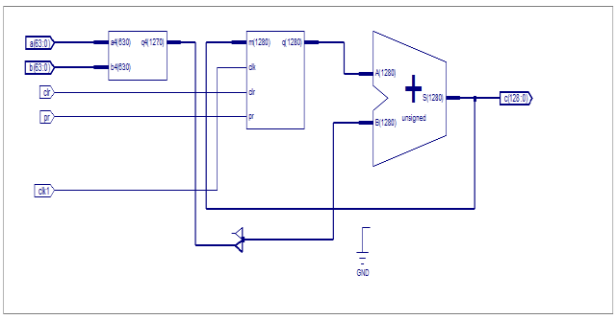
MAC4 Project Status			
Project File:	mac4.ise	Current State:	Synthesized
Module Name:	mac64	• Errors:	No Errors
Target Device:	xc4vfx140-11ff1517	• Warnings:	264 Warnings
Product Version:	ISE 8.1i	• Updated:	Thu 19. May 21:13:53 2016

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	6915	63168	10%
Number of Slice Flip Flops	129	126336	0%
Number of 4 input LUTs	12384	126336	9%
Number of bonded IOBs	260	768	33%
Number of GCLKs	1	32	3%

(a)



(b)



(c)

Fig 5: (a) Design summary of 64-bit MAC unit, (b) Simulation output of 64-bit MAC unit and (c) RTL view of 64-bit MAC unit.

The output of 4-bit, 8-bit, 16-bit, 32-bit and 64-bit Kogge stone adder, 2-bit, 4-bit, 8-bit, 16-bit, 32-bit and 64-bit Vedic multiplier and 2-bit, 8-bit, 16-bit and 64-bit MAC unit is shown in Table 1 and Fig 6:

Table 1: Result of KSA, Vedic Multiplier and MAC Unit

S.No	VIRTEX-4	Proposed KSA Delay (ns)	Proposed Multiplier Delay (ns)	Proposed MAC unit Delay (ns)
1.	2-bit	---	5.773	8.195
2.	4-bit	7.310	8.463	---
3.	8-bit	8.004	11.932	13.236
4.	16-bit	8.616	15.298	18.774
5.	32-bit	11.030	24.394	---
6.	64-bit	12.355	33.324	34.741

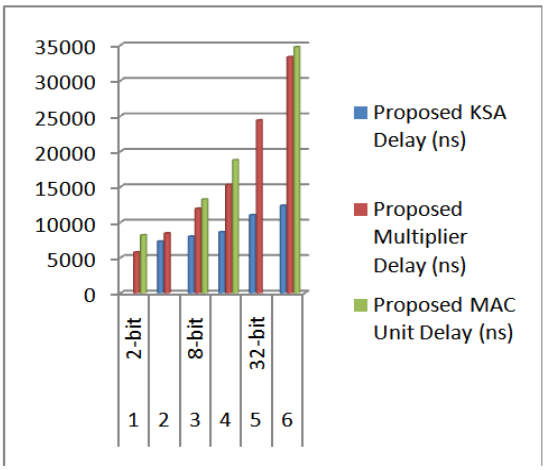


Fig 6: Result of KSA, Vedic Multiplier and MAC Unit using VIRTEX- 4

VI. COMPARISON

In this section, the result of 64-bit MAC unit is compared with the existing MAC unit. Comparison of the MAC unit is done using SPARTAN-3E family, XC3S500 device, FG320 package and -5 speed. The delay of proposed MAC unit is very less compared to the existing design. Comparison is shown in Table 2 and Fig 7:

Table 2: Comparison of delay of 64-bit MAC unit

S.No.	SPARTAN-3E	MAC Unit Delay(ns)[7]	Proposed MAC Unit Delay (ns)
1.	64-bit	325.76	59.705

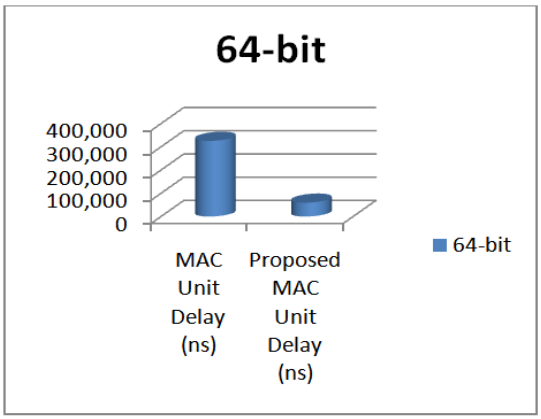


Fig 7: Comparison of delay of 64-bit MAC unit using SPARTAN-3E

VII. CONCLUSION

The proposed design of MAC unit is better than the existing designs as in this the combinational path delay of 64-bit MAC unit is 59.705ns if we are using SPARTAN-3E family and while using VIRTEX-4 family combinational path delay is 34.741ns. Hence the proposed architecture of MAC unit can be used in various DSP applications for fast and better results.

REFERENCES

[1] R.Anitha, Neha Deshmukh, Sarat Kumar Sahoo, S.Prabhakar, Jacob Reglend.I, "A 32 Bit MAC Unit Design Using Vedic Multiplier and Reversible Logic Gate", *International Conference on Circuit, Power and Computing Technologies (ICCPCT), PP 1–6, DOI 10.1109/ICCPCT.2015.7159505*, March 2015.

[2] P.Jagadeesh, S.Ravi, Dr. Kittur Harish Mallikarjun, "Design of High Performance 64 Bit MAC Unit", *International Conference on Circuits, Power and Computing Technologies (ICCPCT), PP 782-786, DOI 10.1109/ICCPCT.2013.6528900*, March 2013.

[3] K.Kalaisrlvi, H. Mangalam, "Area Efficient High Speed and Low Power MAC Unit", *International Journal of Computer Applications, ISSN: 0975 – 8887, Volume-67 Number-23*, PP 40-44, April 2013.

[4] Vijayanath Kunchigi, Linganagouda Kulkarni, Subhash Kulkarni, "32 Bit MAC Unit Design Using Vedic Multiplier", *International Journal of Scientific and Research Publications, ISSN: 2250-3153, Volume-3 Issue-2*, PP 1-7, February 2013.

[5] T.Bhavani, Ms.K.Anuradha, "Design of High Performance 64 bit MAC Unit*", International Journal & Magazine of Engineering Technology Management and Research, ISSN No: 2348-4845,Volume-2, Issue-8*, PP 941-946, August 2015.

[6] Parth S. Patel, Khyati K. Parasania, "Design of High Speed MAC (Multiply and accumulate) Unit Based on Urdhva Tiryakbhyam Sutra", *International Journal of Advanced Research in Computer Engineering & Technology (IJARCET), ISSN: 2278 – 1323, Volume-4, Issue-6, PP 2545-2549*, June 2015

[7] Kandimalla Rajaneesh, M.Bharathi, "A Novel High Performance Implementation of 64-bit MAC Unit and their Delay Comparision",*International Journal of*

Engineering Research & Applications, ISSN 2248-9622, Volume-4, Issue-6, PP 122-127, June 2014.

[8] Shaik.Masthan Sharif1 ,D.Y.V.Prasad2, "Design of Optimized 64 Bit MAC Unit for DSP Applications", *International Journal of Advanced Trends in Computer Science and Engineering, ISSN 2278-3091, Volume-3, Issue-5,* PP 456- 460, October 2014.

[9] Saranya P S, Veena Chandran M, Keerthana P, Aravind S, Prajitha P Nair, Archana Thulaseedharan, "Implementation and Performance Comparision of Modified Booth Multiplier by Using Diffferent Adder Techniques", *International Journal of Engineering Science & Innovative Technology, ISSN 2319-5967, Volume-4, Issue-2,* PP 321-327, March 2015.